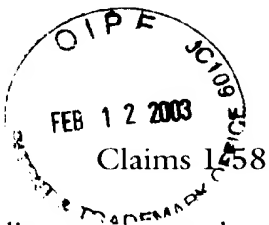

REMARKS/ARGUMENTS

Claims 1-58 are pending in the application. Claims 1-58 stand rejected. Applicants reserve the right to pursue the original claims and alter the claims in this application and in other applications.

Claims 1-28 and 42-58 stand rejected under 35 U.S.C. §102(e) as being anticipated by Lowrey et al. Claim 1 recites, inter alia, "first and second programmable conductor memory elements for storing complementary binary digit values". Claim 14 also recite complementary binary digit values. Such a feature is neither disclosed nor suggested by Lowrey, nor any of the prior art cited in the Office Action. For at least the above reasons, the rejection of claims 1, 14, and all claims dependent therefrom should be withdrawn.

Claim 42 (as amended) now recites, inter alia, "storing a binary value as respective complementary resistance states in a first and second programmable conductor memory element". Claim 53 (as amended) now recites, inter alia, "forming first and second complementary conductor memory elements arranged to store complementary logic states". Such a feature is neither disclosed nor suggested by Lowrey, or any of the prior art cited in the Office Action. For at least the above reasons, the rejection of claims 42, 53 and all claims dependent therefrom should be withdrawn.

Claims 29-41 stand rejected under 35 U.S.C. §103 as being unpatentable over Lowrey. Claim 29 recites "first and second programmable conductor memory elements for storing complementary binary digit values". Such a feature is neither disclosed nor

suggested by Lowrey nor any of the prior art cited in the Office Action. For at least the above reasons, the rejection of claim 29 and all claims dependent therefrom should be withdrawn.

A new claim 59 has been added which is similar to claim 53, but which recites a "circuit for operating said access transistors" instead of the "row lines for operating said access transistors" as recited in claim 53. Claim 59 is also distinguishable over Lowrey.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: February 12, 2003

Respectfully submitted,

By_____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Please amend claims 42 and 53 as follows.

42. (Amended) A method of operating a programmable conductor memory device comprising:

storing a binary value as respective [different] complementary resistance states in a first and second programmable conductor memory element;

determining a binary value stored in one of said memory elements by discharging respective voltages through said memory elements and comparing the discharging voltages.

53. (Amended) A method of producing a programmable conductor memory device, said method comprising;

forming first and second digit lines;

forming first and second programmable conductor memory elements arranged to store complementary logic states;

forming first and second access transistors for respectively coupling said first and second memory elements to said first and second digit lines;

forming a precharge circuit for precharging said first and second digit lines to a first voltage;

forming respective row lines for operating said access transistors to couple said memory elements to respective digit lines; and

forming a sense amplifier which has inputs respectively coupled to said digit lines.

Please add the following new claim.

59. (Newly Added) A method of producing a programmable conductor memory device, said method comprising;

forming first and second digit lines;

forming first and second programmable conductor memory elements arranged to store complementary logic states;

forming first and second access transistors for respectively coupling said first and second memory elements to said first and second digit lines;

forming a precharge circuit for precharging said first and second digit lines to a first voltage;

forming a circuit for operating said access transistors to couple said memory elements to respective digit lines; and

forming a sense amplifier which has inputs respectively coupled to said digit lines.